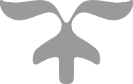


DLD Lab-09

Multiplexer & De Multiplexer



NATIONAL UNIVERSTIY OF COMPUTER AND EMERGING SCIENCES, FAST- Peshawar Campus

Department Of Computer Science

Instructor: Engr. Waseem Ullah

EL1005 – Digital Logic Design-Lab

SEMESTER SPRING 2022

Contents

[1. Objectives: 2](#_Toc74849008)

[2. Equipment Required: 2](#_Toc74849009)

[3. Background Theory 2](#_Toc74849010)

[4. 4x1 Mux Contd. 3](#_Toc74849011)

[5. 4x1 Mux(74LS153 Testing in Multisim) 4](#_Toc74849012)

[6. 8x1 Mux 4](#_Toc74849013)

[7. 8x1 Mux(74LS151 Testing in Multisim) 5](#_Toc74849014)

[8. DE Multiplexer 6](#_Toc74849015)

[9. 1x4 De Multiplexer 6](#_Toc74849016)

[10. 1x4 De-Mux(74LS139 Testing in Multisim) 7](#_Toc74849017)

[11. 1x8 De Multiplexer 8](#_Toc74849018)

# Objectives:

* Design and implement the circuitry for a 4 to 1 Multiplexer.
* Test the functionality of a 1x4 DE multiplexer using the IC-74LS139
* Test the functionality of a 8x1 multiplexer using the IC-74LS151
* Test the functionality of a 4x1 multiplexer using the IC-74LS153Gaining a close insight into the functioning and properties of multiplexer (MUX) circuits
* Developing skills in the design and testing of combinational logic circuits.

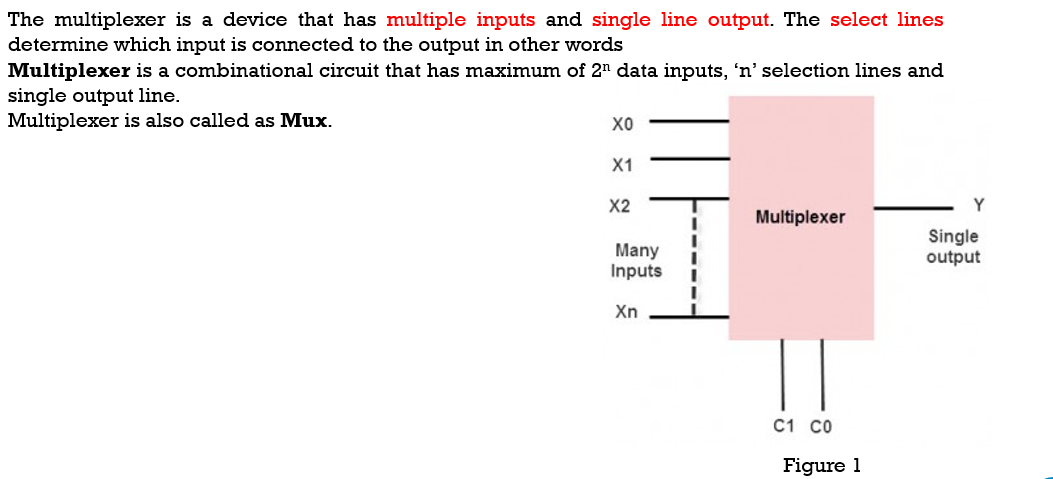
# Equipment Required:

* DEV-2765E Trainer Board/ Multisim 14.2 /Logic.ly
* 74LS04 Hex Inverter
* 74LS08 And gate
* 74LS32 OR gate
* 74LS151 (8-to-1 Multiplexer)
* 74LS153 (dual 4-to-1 Multiplexer)

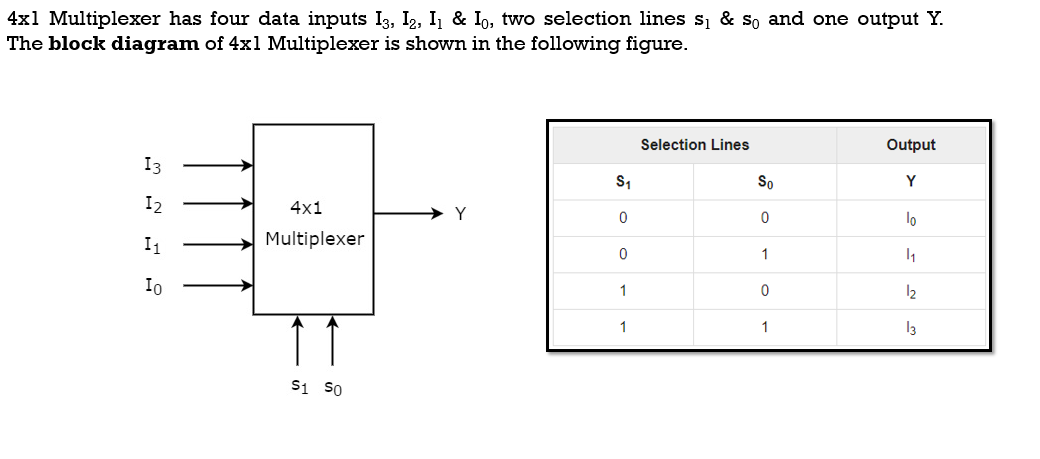
# Background Theory

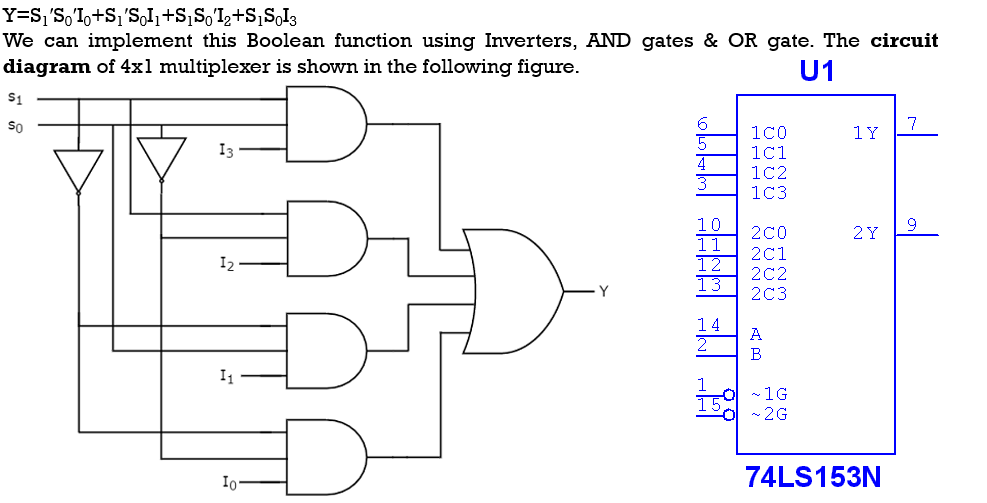
A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. The selection of a particular input line is controlled by a set of input variables, called selection input. Normally, there are 2n input lines and n selection inputs whose bit combination determines which input is selected.

A de multiplexer is doing the opposite function of multiplexer. It takes input on a single input line and the select lines determines one of the 2n output lines and the input contents is visible on that particular output.

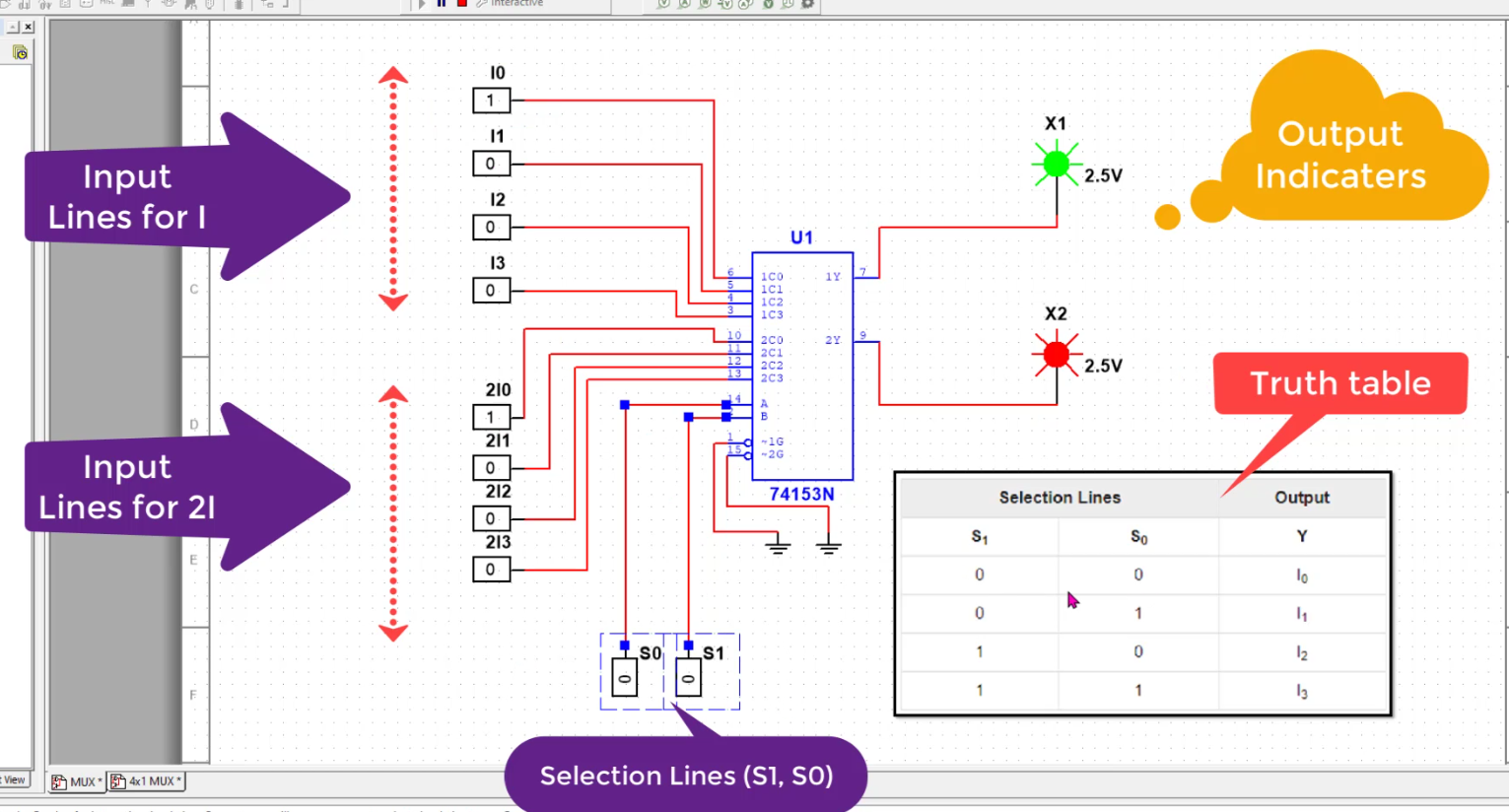


# 4x1 Mux Contd.

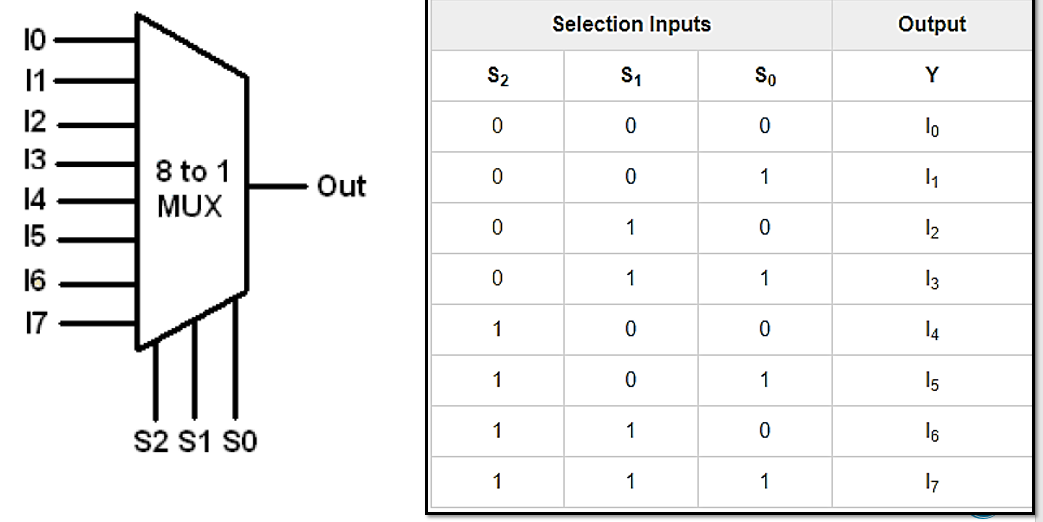


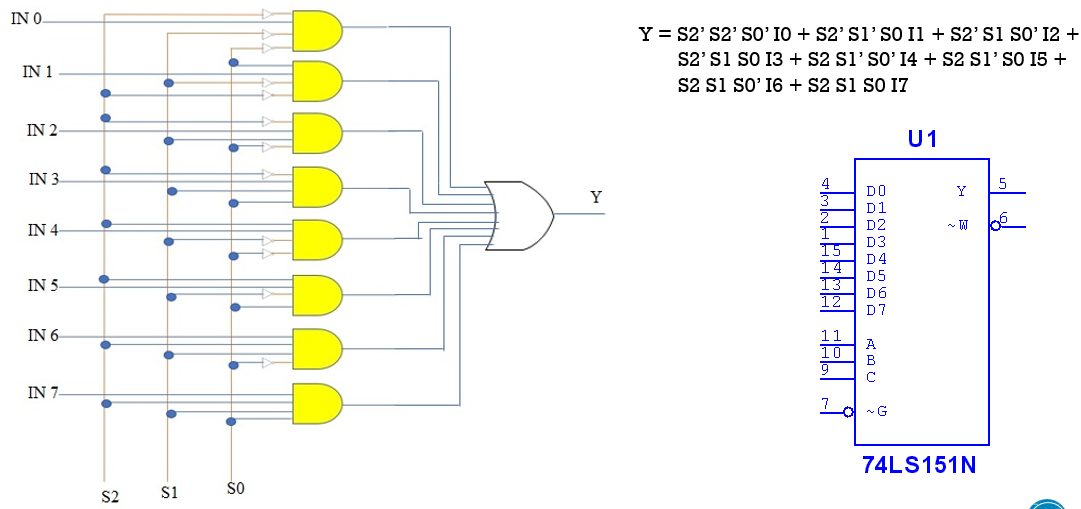


# 4x1 Mux(74LS153 Testing in Multisim)

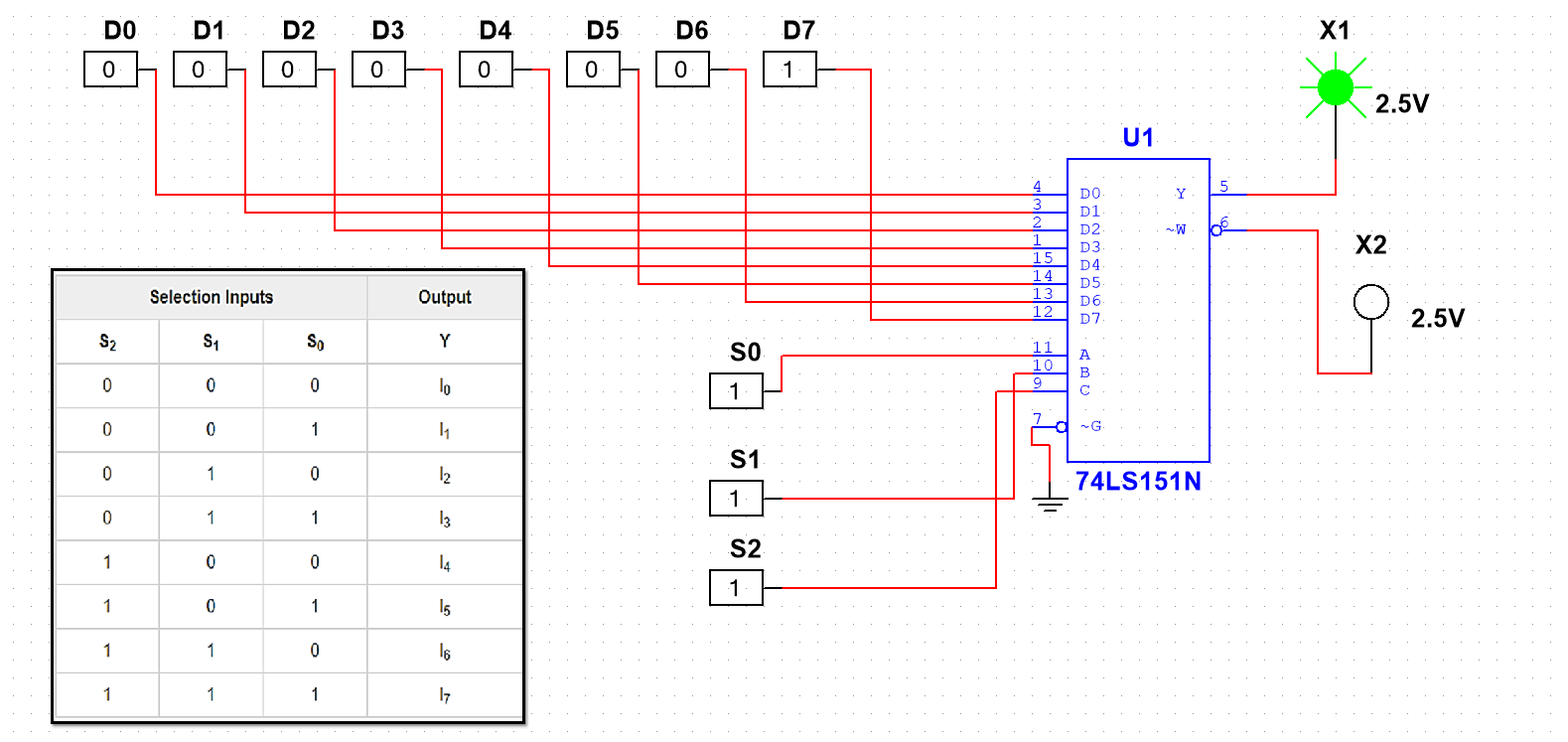


# 8x1 Mux

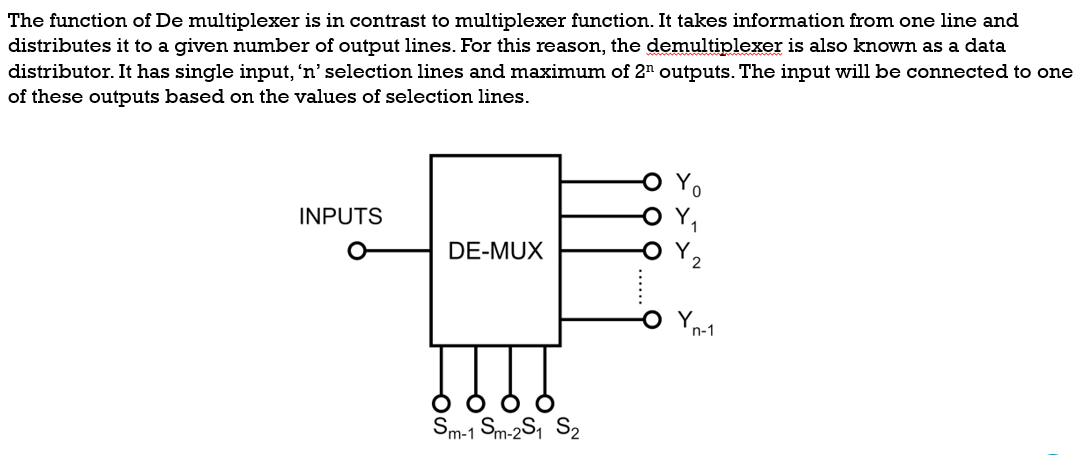




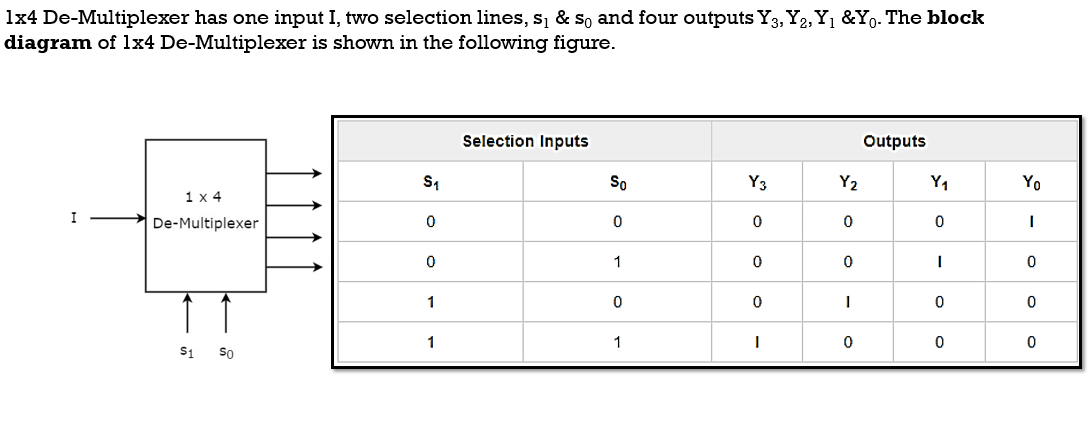
# 8x1 Mux(74LS151 Testing in Multisim)

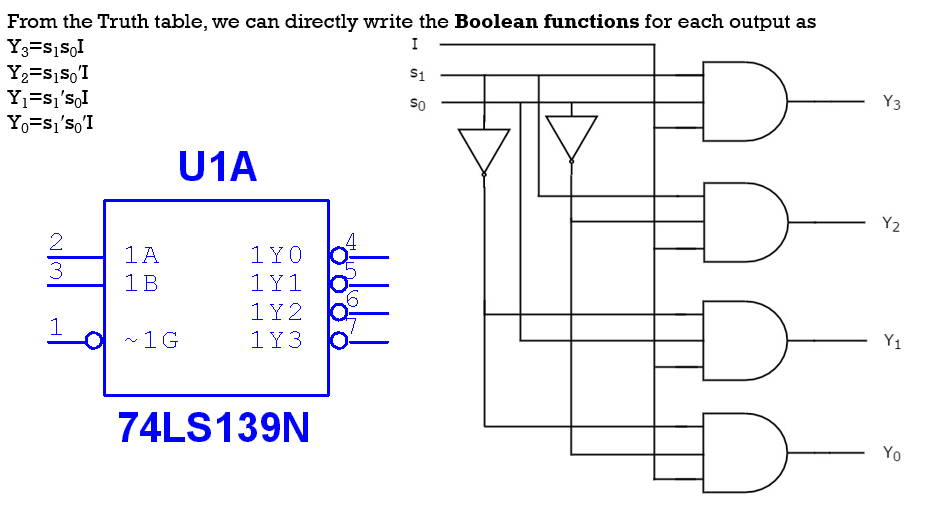


# DE Multiplexer

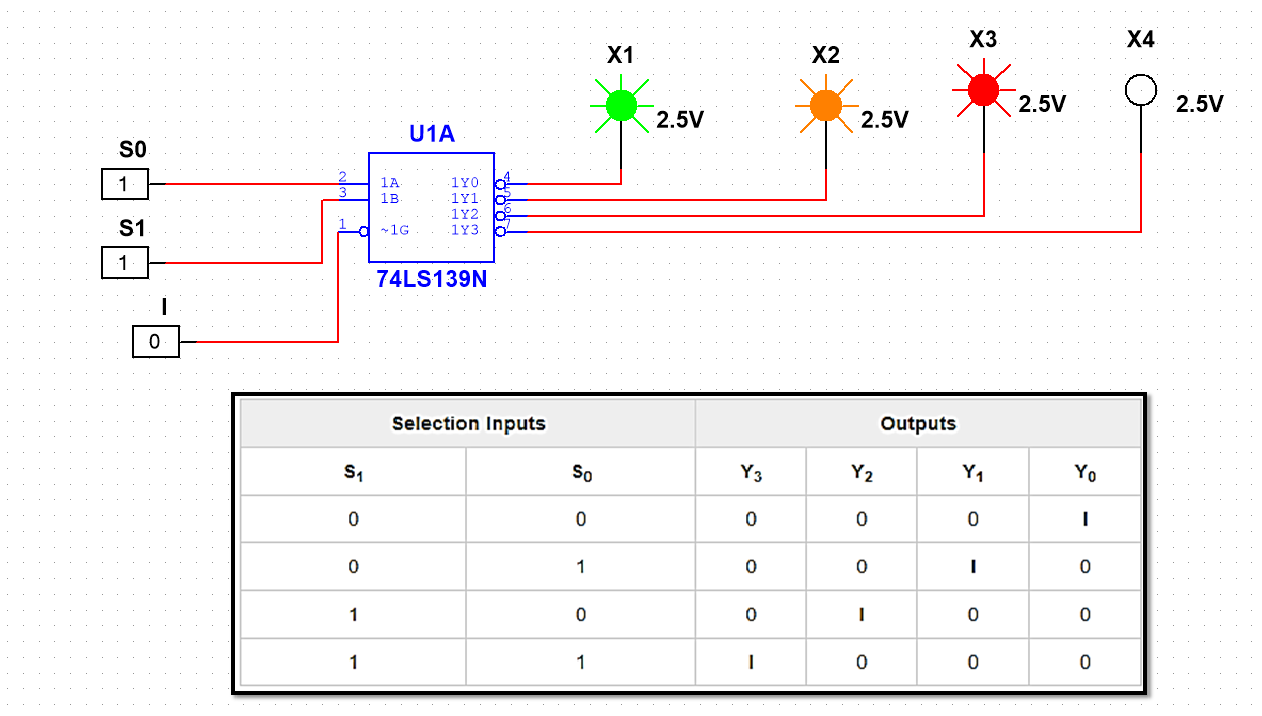


# 1x4 De Multiplexer





# 1x4 De-Mux(74LS139 Testing in Multisim)



# 1x8 De Multiplexer

